Amendments to the Drawings:

The office action states in part:

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because:

a) the specification does not include the following reference sign mentioned in the drawings:

i) In Fig. 11c, reference numeral "1200c" are not disclosed in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Since applicant has not responded or amended to the objection in the above paragraph, the objection is maintained.

Applicants have amended the specification to include the disclosure of reference number "1200c." Accordingly, Applicants submit that no amendment to the drawings is needed.

REMARKS

Claims 1-8 are pending. Claims 1-8 are rejected. Claims 1 and 8 amended.

Claim Objections

The Office Action states in part:

Claim 8 is objected to because of the following informalities:
(A) In claim 8, line 2, "said solder mask" should be-- a solder mask --.
Appropriate correction is required.

§ 102 Rejections

Claims 1, 4 and 5 stand rejected under 35 USC § 102(b) as being anticipated by Wensel et al. (U.S. Pat. No. 6,291,899).

The Office Action states in part:

Regarding claim 1, Wensel et al. discloses in e.g., Fig. 4A a laminated flip-chip interconnect package (a package 36 in Fig. 4A and column 4, line 46) comprising

- a substrate (24; column 3, lines 38-39) having a chip attach surface (the top surface of the substrate 24 where the chip 26 is attached) and an opposing board attach surface (the bottom surface of the substrate 24; column 4, lines 64-65) that define contact pads (the pads between the solder ball 38 and the substrate 24, and pads on the top surface of the substrate 24 that are connected to the wire 30) for attachment to corresponding pads on the chip (26; column 3, line 40) and board (board; column 4, lines 64-65),
- wherein the board attach surface (at the bottom surface of the substrate 24) comprises
  - o contact pads (the pads between the solder ball 38 and the substrate 24, and pads on the top surface of the substrate 24 that are connected to the wire 30) opposite a chip attach location and regions "adjacent" the chip attach location on the chip attach surface except at least one solid plane area (at the area of the element 44; column 4, line 46) of the board attach surface,
  - o said area (at the area of the element 44) being opposite a chip attach surface region adjacent a corner of chip (see Fig. 4A), and
- said board attach surface comprising a dielectric material (44; column 5, lines 5-7).

Regarding claim 4, Wensel et al. discloses in e.g., Fig. 4A a laminated flip-chip interconnect package (a package 36 in Fig. 4A and column 4, line 46) comprising

- a substrate (24; column 3, lines 38-39) having a chip attach surface (the top surface of the substrate 24 where the chip 26 is attached) and an opposing board attach surface (the bottom surface of the substrate 24; column 4, lines 64-65) that define contact pads (the pads between the solder ball 38 and the substrate 24, and pads on the top surface of the substrate 24 that are connected to the wire 30) for

attachment to corresponding pads on the chip (26; column 3, line 40) and board (board; column 4, lines 64-65),
- wherein the board attach surface (at the bottom surface of the substrate 24) comprises
o at least one solid plane area (at the area of the element 44; column 4, line 46),
o said area (at the area of the element 44) being opposite a chip attach surface region adjacent at least one corner of a chip attach location (see Fig. 4A), and
- said board attach surface comprising a metal (44; column 5, lines 5-7).
Regarding claim 5, Wensel et al. discloses in e.g., Fig. 4A said metal being copper (copper 44; column 5, lines 5-7).

Applicants respectfully submit that according to MPEP 2131 "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (citing *Verdegall Bros. V. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)).

Applicants have amended claim 1 to clarify that the solid plane area is a discontinuity in the pattern of contact pads of the board attach surface. This clarification does not narrow the scope of claim 1. The discontinuity may be created by, for example, an absence of contact pads or a planar material over a portion of the pads. *See, e.g.*, spec. at p. 14, lines 10-22.

Wensel does not disclose a pattern of contact pads opposite and adjacent to a chip attach location on the chip attach surface except at least one solid plane area on the board attach surface, said solid plane area being adjacent to a corner of a chip attach location. Accordingly, the reference does not describe every element of the claimed invention.

Based on the foregoing, Applicant(s) submit that the cited reference cannot support a 35 U.S.C. 102(b) rejection and respectfully requests that the rejection be withdrawn.

§ 103 Rejections

Claims 2, 3 and 6-8 stand rejected under 35 USC § 103(a) as being unpatentable over Wensel et al. in view of Jacobs (U.S. Pat. No. 6,294,407).

The Office Action states in part:

Regarding claims 2, 3, 6 and 7, while Wensel et al. discloses the use of the solid material (i.e., the dielectric or metal) on a solid plane area, Wensel et al. does not disclose a coverlay material. Jacobs teaches in e.g., Fig. 8 a solid material on a solid plane area (810; column 11, lines 28) being covered with a layer of a coverlay material (epoxy 130; column 7, lines 55-58).
It would have been obvious to one of ordinary skill in the art at the time when

the invention was made to apply the coverlay material (e.g., epoxy) to cover the solid material (e.g., the dielectric or metal) on the solid plane area of Wensel et al. as taught by Jacobs to prevent short circuits between conductive bumps (column 8, lines 2-4).

Regarding claim 8, Wensel et al, as modified, discloses a solder mask (130 of Jacobs) having a plurality of openings (132 of Jacobs) defining ball grid array pads.

Applicants respectfully submit that according to MPEP 2142, to establish a case of prima facie obviousness, three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references or generally known to one skilled in the art, to modify or combine reference teachings, 2) there must be reasonable expectation of success, and 3) prior art references must teach or suggest all the claim limitations. The ability to modify the method of the references is not sufficient. The reference(s) must provide a motivation or reason for making the changes. *Ex parte Chicago Rawhide Manufacturing Co., 226 USPQ 438 (PTO Bd. App. 1984).*

Applicants respectfully submit that the references cannot support a case of *prima facie* obviousness as to the claims because, among other possible reasons, the cited references do not provide a motivation or suggestion for a pattern of contact pads opposite and adjacent to a chip attach location on the chip attach surface except at least one solid plane area on the board attach surface, said solid plane area being adjacent to a corner of a chip attach location because Wensel teaches the use of stabilizing plates that surround the periphery of the conductive bump area (plate 34 in Figs. 3A and 3B; *see also* Wensel at col. 4, lines 21-23) or that are interlaced between the conductive bumps (plate 44 in Figs. 4A and 4B; *see also* Wensel at col. 4, lines 51-54). The combination of Jacobs with Wensel does not make up for the deficiencies of Wensel as a prior art reference. In addition, these references do not disclose all the elements of the present invention because they do not disclose a pattern of contact pads opposite and adjacent to a chip attach location on the chip attach surface except at least one solid plane area on the board attach surface, said solid plane area being adjacent to a corner of a chip attach location.

For these reasons, Applicant(s) submit that the cited references will not support a 103(a) rejection of the claims invention and request that the rejection be withdrawn.

In addition to the foregoing arguments, Applicant(s) submit that a dependent claim should be considered allowable when its parent claim is allowed. *In re McCairn*, 1012 USPQ 411

(CCPA 1954). Accordingly, provided the independent claims are allowed, all claims depending therefrom should also be allowed.

Based on the foregoing, it is submitted that the application is in condition for allowance. Withdrawal of the rejections under 35 U.S.C. 102 and 103 is requested. Examination and reconsideration of the claims are requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant(s)' attorney if the Examiner believes any remaining questions or issues could be resolved.

Respectfully submitted,

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Date

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